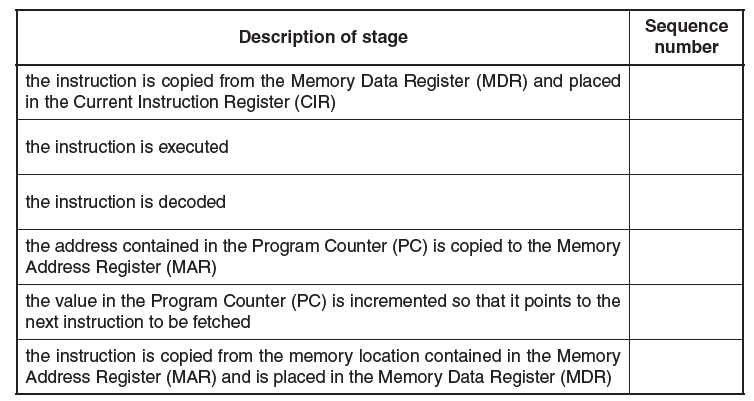
**5.3 fetch-execute cycle**

**Name \_\_\_\_\_\_\_\_\_\_\_ class\_\_\_\_\_\_\_\_\_\_\_\_\_**

**1**

The table shows six stages in the von Neumann fetch-execute cycle.

Put the stages into the correct sequence by writing the numbers 1 to 6 in the right hand column.



**2**

**(a)** Describe how special purpose registers are used in the fetch stage of the fetch-execute cycle.

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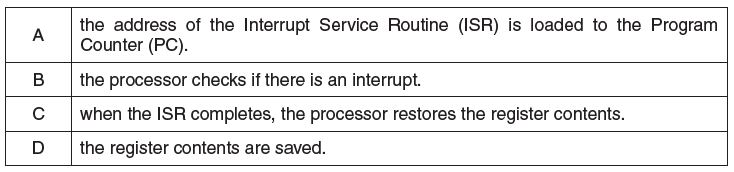
\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(b)** Use the statements A, B, C and D to complete the description of how the fetch-execute cycle handles an interrupt.



At the end of the cycle for the current instruction\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ .

If the interrupt flag is set, \_\_\_\_\_\_\_\_\_\_\_\_\_,\_\_\_\_\_\_\_\_\_\_\_\_and \_\_\_\_\_\_\_\_\_\_\_\_\_\_

The interrupted program continues its execution.

**3**

A student has written the steps of the fetch stage of the fetch-execute (FE) cycle in register transfer

notation. The student has made some errors.

Line 1 MDR [PC]

Line 2 PC PC + 1

Line 3 MDR [MAR]

Line 4 CIR PC

**(a)** Identify the line numbers of **three** errors that the student has made. Write the correct notation for each error.

**Line number of error Correct notation**

**(b)** One stage of the FE cycle includes checking for interrupts.

**(i)** Give **three** different events that can generate an interrupt.

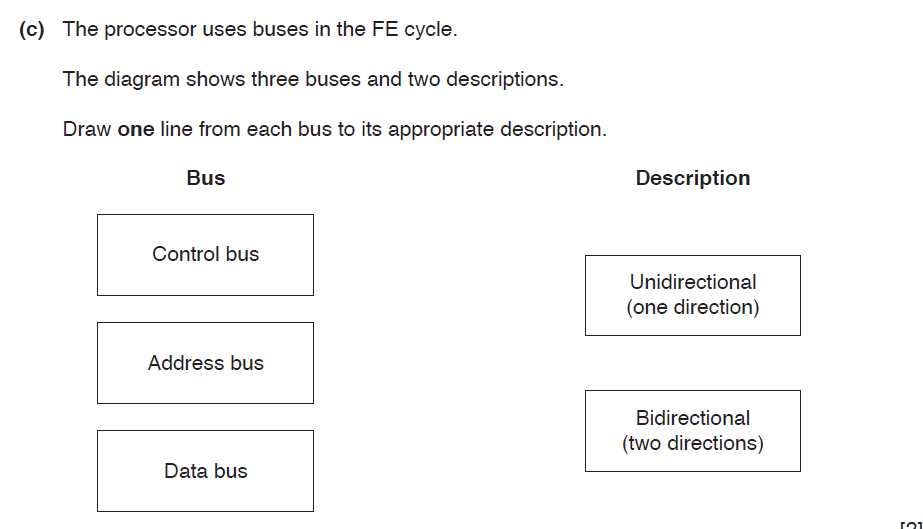
1 ....................................................................................................................................

2 ....................................................................................................................................

3 .....................................................................................................................................

**(ii)** Explain how interrupts are handled during the fetch-execute cycle.

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**4**

The Von Neumann model uses a series of registers.

**(a)** Explain what is meant by the term **register**.

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**(b) (i)** Explain the purpose of the Memory Data Register (MDR).

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**(ii)** Name **two** registers, other than the MDR, that are used in the fetch-execute cycle.

Register1

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Register2

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**(c)** X is a register. The current contents of X are:

1 0 0 0 0 1 1 1

**(i)** The current contents of register X represent an unsigned binary integer.

Convert the value in X into denary.

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**(ii)** The current contents of register X represent a Binary Coded Decimal.

Convert the value in X into denary.

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**(iii)** The current contents of register X stores a two’s complement binary integer.

Convert the value in X into denary.

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**5**

The sequence of operations shows, in register transfer notation, the fetch stage of the fetchexecute

cycle.

1 MAR ←[PC]

2 PC ←[PC] + 1

3 MDR ←[[MAR]]

4 CIR ←[MDR]

• [register] denotes contents of the specified register or memory location

• step 1 above is read as “the contents of the Program Counter are copied to the Memory

Address Register”

**(i)** Describe what is happening at step 2.

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**(ii)** Describe what is happening at step 3.

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**(iii)** Describe what is happening at step 4.

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**(c)** Describe what happens to the registers when the following instruction is executed:

LDD 35

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**(d)**

**(i)** Explain what is meant by an interrupt.

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...................................................................................................................................... **(ii)** Explain the actions of the processor when an interrupt is detected.

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